

***1.***

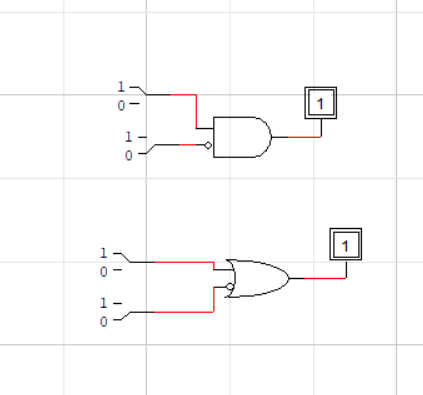
The First circuit is of **3 input AND gate**.

|  |  |  |  |
| --- | --- | --- | --- |
| Intput 1 (A) | Input 2 (B) | Input 3 (C) | Output X |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

***2.***

The Second circuit is of **3 input OR gate**.

|  |  |  |  |
| --- | --- | --- | --- |
| Intput 1 (A) | Input 2 (B) | Input 3 (C) | Output X |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |



***1.***

The First circuit is of **2 input AND gate (1 inv)**.

|  |  |  |  |
| --- | --- | --- | --- |
| Intput 1 (A) | Input 2 (B) | Input 2 B(inverted) | Output X |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |

When 2 inputs are inputted in the AND GATE(1-inv), then one of them is inverted before being inputted in the logic gate.

***2***.

The second circuit is of **2 input OR gate (1 inv)**.

|  |  |  |  |
| --- | --- | --- | --- |
| Intput 1 (A) | Input 2 (B) | Input 2 B(inverted) | Output X |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |

When 2 inputs are inputted in the OR GATE(1-inv), then one of them is inverted before being inverted in the logic gate.